

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

D. Remarks

Rejection of Claims 1, 2-3, 6-7, 21-24, and 26-27 Under 35 U.S.C. §102(e) based on Hung et al. (USPAP 2002/0132403).

5 The rejection of claims 1, 2-3, and 6-7 will first be addressed.

Claim 1 has been re-written to include all the elements of allowed claim 29.

The rejection of claims 21-24 and 26-27 will now be address.

10 The semiconductor device of amended claim 21 includes a first transistor formed in a first region. The first transistor includes a first upper layer gate electrode formed on and in electrical connection with a first corresponding lower layer gate electrode. A first insulating film is formed on a majority of a side surface of the first lower layer gate electrode. A second insulating film is formed on a side surface of the first upper layer gate electrode. The second insulating film has a lower thermal growth rate with respect to the first upper layer gate electrode material than the
15 thermal growth rate of the first insulating film with respect to the first lower layer gate electrode material. A first etching stopper is formed on the outside of the first and second insulating films and in contact with a majority of an outside surface of the first insulating film formed on the majority of the side surface of the first lower layer gate electrode. The second insulating film has a thickness of less than 6 nm.

20 *Hung et al.* discloses an IGFET having a cap film 8, a metal silicide layer 6a (alleged to correspond to Applicant's first upper gate electrode of claim 21)¹, and a polysilicon layer 6. The IGFET includes a silicon dioxide layer 10 (alleged to correspond to Applicant's first insulating film of claim 21)², a nitride liner layer 12 (alleged to correspond to Applicant's second insulating film)³, and a borderless nitride layer 20 (alleged to correspond to Applicant's first etching
25 stopper)⁴. However, in *Hung et al.*, borderless nitride layer 20 is not formed in contact with a majority of the outside surface of silicon dioxide layer 20 formed on the majority of the side surface of polysilicon layer 6 and therefore these elements cannot correspond to the "first etching

¹ See the Final Office Action, dated 5/13/05, Page 3, 3rd paragraph.

² See the Final Office Action, dated 5/13/05, Page 3, 3rd paragraph.

³ See the Final Office Action, dated 5/13/05, Page 3, 3rd paragraph.

⁴ See the Final Office Action, dated 5/13/05, Page 3, 3rd paragraph.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

stopper and the first insulating film” of Applicant’s amended claim 21. As noted above, claim 21 recites the first etching stopper is formed on the outside of and in contact with a majority of the first insulating film. This is illustrated in more detail below:

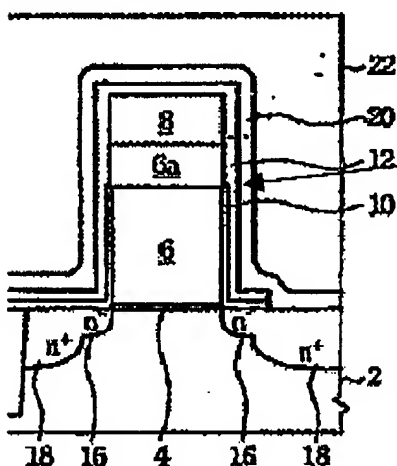


FIG. 5 of *Hung et al.* showing a liner layer 12 interposed between silicon oxide layer 10 and borderless nitride layer 20.

Thus, borderless nitride layer 20 is not “in contact with a majority of” silicon oxide layer 10.

Accordingly, because the reference *Hung et al.* does not show all elements of amended claim 21, this ground of rejection is believed to be traversed.

10 Rejection of Claims 2-3, 6-7, 21-24, 26-27 Under 35 U.S.C. §103(a), based on *Hung et al.*

Claim 1 has been amended to include the elements of allowed claim 29. Therefore, the rejection of claims 2-3 and 6-7 is moot.

The rejection of claims 21-24 and 26-27 will now be addressed.

15 As is well known, in proceedings before the Patent and Trademark Office, the examiner bears the burden of establishing a prima facie case of obviousness based on the prior art.⁵ In addition, to establish a prima facie case of obviousness, a rejection must meet three basic criteria. First, there must be some suggestion or motivation to modify a reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art
20 reference(s) must teach or suggest all claim limitations.⁶

⁵ *Ex parte Obukowicz*, 27 USPQ 1063, 105 (B.P.A.I. 1992).

⁶ MPEP §2143.

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

To address the rejection of claims 21-24, 26, and 27, the arguments set forth above with respect to claim 21 are incorporated herein by reference. Namely, *Hung et al.* does not show or suggest a first etching stopper is formed on the outside of the first and second insulating films and in contact with a majority of a first insulating film. Accordingly, the cited reference does not show or suggest all the limitations of claim 21.

Further, because the reference intentionally introduces an interposing liner layer 12 that prevents such direct contact between silicon oxide layer 10 and borderless nitride layer 20, the reference not only does not suggest such an arrangement, but is believed to teach away from the limitations of amended claim 21.

Accordingly, a prima facie case of obviousness is not believed to exist for this claim, and this ground of rejection is traversed.

Rejection of Claims 5 and 25 Under 35 U.S.C. §103(a), based on *Hung et al.* in view of *Liaw* (USP 6,448,140).

Claim 1 from which claim 5 depends has been amended to include all the elements of allowed claim 29. Thus, the rejection of claim 5 is now moot.

Claim 25 depends from claim 21 and recites that the first lower layer gate electrode has a greater length than the first upper layer gate electrode.

To the extent the rejection relies on *Hung et al.*, the arguments set forth above with respect to claim 21 are incorporated herein by reference. Namely, *Hung et al.* does not show or suggest a first etching stopper formed on the outside of the first and second insulating films and “in contact with a majority of an outside surface of the first insulating film formed on the majority of the side surface of the first lower layer gate electrode”.

Further, as is also well established, a prima facie case of obviousness may be rebutted by showing that the art, in any material respect, teaches away from the claimed invention.⁷

As noted in Applicant's previous response, *Liaw* is believed to teach away from the invention of claim 21 from which claim 25 depends. Claim 21 includes a “second insulating film

⁷ *In re Geisler*, 43 USPQ2d 1362, 1366 (Fed. Cir. 1997).

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

formed on a side surface of the first upper layer gate electrode". The second insulating film has a lower thermal growth rate with respect to the first upper layer gate electrode material than the thermal growth rate of the first insulating film with respect to the first lower layer gate electrode.

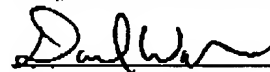
5 *Liaw* show the opposite of Applicant's claim limitations. *Liaw* discloses a silicon oxide film 9c formed on a side surface of an upper tungsten silicide layer 3, as well as a silicon oxide film 9b formed on the sides of a lower polysilicon layer 3. However, the upper layer silicon oxide film 9c having a higher growth rate than the lower silicon oxide film 9b.

Thus, even if a prima facie case could be established, the teachings of the cited reference *Liaw* would rebut any such case.

10 For all of these reasons, this ground of rejection is traversed.

Claims 1, 21, and 28 have been amended. Claim 29 has been cancelled. Claim 1 has been amended to include all the elements of claim 29, which was indicated as allowable. Claim 28, which was indicated as allowable, has been re-written in independent form including all
15 elements of claims 21, 26, and 27. The present claims 1-3, 5-7 and 17-28 are believed to be in allowable form. It is respectfully requested that the application be forwarded for allowance and issue.

Respectfully Submitted,

20  July 7, 2005
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